TABLE 1. Assembly and packaging – difficult near-term challenges.

DIFFICULT CHALLENGES 32 nm	SUMMARY OF ISSUES
Impact of BEOL, including Cu/low k on packaging	■ Direct wirebond and bump to Cu or improved barrier systems bondable pads ■ Bump and underfill technology to assure low K dielectric integrity including lead-free solder bump system ■ Improved fracture toughness of dielectrics ■ Interfacial adhesion ■ Reliability of first-level interconnect with low K ■ Mechanisms need to be developed to measure critical properties ■ Probing over copper/low K
Wafer-level CSP	■ Reductions in I/O pitch for small die with high pin count ■ Solder joint reliability and cleaning processes for low stand-off ■ Wafer thinning and handling technologies ■ Compact ESD structures ■ TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	■ Mixed signal co-design and simulation environment ■ Rapid turnaround modeling and simulation ■ Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis ■ Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/ current and lower voltage switching) ■ System level co-design is needed now ■ EDA for "native" area array is required to meet the Roadmap projections ■ Models for reliability prediction
Embedded components	■ Low-cost embedded passives: R, L, C ■ Embedded active devices ■ Quality levels required not attainable on chip
Thinned die packaging	■ Wafer-level embedded components ■ Wafer/die handling for thin die ■ Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact ■ Establish infrastructure for new value chain ■ Establish new process flows ■ Reliability ■ Testability ■ Different active devices ■ Electrical and optical interface integratio
Close gap between chip and substrate – improved organic substrates	■ Increased wireability at low cost ■ Improved impedance control and lower dielectric loss to support higher frequency applications ■ Improved planarity and low warpage at higher process temperatures ■ Low moisture absorption ■ Increased via density in substrate core ■ Alternative plating finish to improve reliability ■ Solutions for operation temp up to C5 interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology) ■ Production techniques will require silicon-like production and process technologies after 2005 ■ Tg compatible with Pb-free solder processing (including rework @260°C)