TABLE 1. Laminates typically specified.

	TODAY	12-18 MOS.
Rigid (FR-4)	87.3%	84.8%
Standard multilayer	67.2%	65.2%
CEM	8.6%	9.0%
High-performance multilayer	50.4%	58.2%
Paper	2.0%	1.6%
Flexible (polyimide or polyester)	28.7%	30.3%
Rigid-flex (including multilayer rigid-flex)	25.0%	27.0%
Don't know	0.8%	2.5%

Respondents were asked to check all that apply.

TABLE 2. Typical laminate Tg.

	TODAY	12-18 MOS.
Tg <150°C	14.8%	9.0%
Tg 150°C to 170°C	33.6%	22.5%
Tg 170°C to 200°C	27.9%	40.2%
Tg >200°C	9.0%	11.5%
Don't know	14.8%	16.8%

Respondents were asked to check all that apply.

TABLE 3. Conductor widths and spacings.

	TODAY	12-18 MOS.
0.001/0.001"	2.9%	3.3%
0.002/0.002"	4.9%	9.4%
0.003/0.003"	18.4%	29.9%
0.004/0.004" - 0.006/0.006"	57.0%	60.7%
0.006/0.006" - 0.008/0.008"	50.0%	46.3%
0.008"/0.008" or above	45.1%	40.6%
Don't know	4.5%	6.6%

Respondents were asked to check all that apply.

TABLE 4. Copper foil thicknesses.

	TODAY	12-18 MOS.
Semi-additive copper	1.2%	3.3%
⅛ oz.	5.7%	6.1%
¼ oz.	14.3%	18.9%
⅜ oz.	10.7%	13.1%
½ oz.	70.5%	70.1%
1 oz.	69.3%	66.8%
1 to 5 oz.	43.9%	43.4%
More than 5 oz.	4.1%	6.1%
Don't know	7.4%	9.4%

Respondents were asked to check all that apply.

TABLE 5. Typical layer counts.

	TODAY	12-18 MOS.
Single-sided	20.9%	20.1%
Double-sided	59.8%	57.4%
4 to 6 layers	75.0%	74.2%
8 to 10 layers	57.4%	61.1%
12 to 18 layers	38.5%	44.3%
18 to 24 layers	17.2%	21.3%
More than 24 layers	8.6%	9.8%
Don't know	0%	1.6%

Respondents were asked to check all that apply.

TABLE 6. Advanced fabrication techniques.

	TODAY	12-18 MOS.
Chip carriers (single and multiple)	21.3%	21.7%
Microvias (0.005 or less)	34.0%	52.5%
Blind vias (any type)	47.5%	56.6%
Buried vias (filled and unfilled)	40.6%	48.4%
Impedance-controlled boards	66.8%	70.9%
Backdrilling	13.5%	17.6%
Embedded passives	11.1%	24.6%
None of the above	19.3%	13.1%

Respondents were asked to check all that apply.

TABLE 7. PCB metallic finishes.

	TODAY	12-18 MOS.
Copper only (OSP)	22.5%	23.0%
HASL	55.3%	40.6%
Lead-free HASL	23.0%	37.3%
SnPb plate and reflow	18.9%	12.3%
Im. Sn	18.0%	18.9%
SnNi	7.0%	6.1%
Electroplated NiAu	29.5%	31.6%
ENIG	59.0%	59.4%
Im. Ag	27.5%	34.4%
Other	0.8%	2.0%
Don't know	1.2%	4.1%

Respondents were asked to check all that apply.

TABLE 8. Minimum passive size.

	TODAY	12-18 MOS.
01005	0%	2.9%
0201	15.2%	27.9%
0402	56.1%	51.2%
0603	23.4%	10.2%
0804	1.6%	1.6%
1206	1.6%	1.6%
Don't know	2.0%	4.5%

TABLE 9. Bare PCB Acceptance Rate

>95%	64.3%
90-95%	21.3%
80-90%	11.5%
70-80%	2.0%
60-70%	0.0%
<60%	0.8%

TABLE 10. Common Bare Board Defects

Laminate (pits, dents, bow/twist, delamination, measling, registration)	38.9%
Solderability	31.6%
Plating	28.7%
Surface finishes (poor coverage, etc.)	26.2%
Electrical (crosstalk, impedance, etc.)	25.0%
Drilling (burrs, nailheading, misregistration, pad tearout, wedge voids, pink ring)	20.5%
Cleanliness	18.9%
Legend/screen (misprints, etc.)	15.6%
Missing conductors/pads	7.8%

Respondents were asked to check all that apply.