

TABLE 1. Timing formulas and parameters for a common-clock bus.

EQUATION 1

$$T_{su_mrg} = [T_{cyc} - T_{co_dq,max} - (T_{pcb_skw,max} + T_{clk_skw,max} + T_{jtr}) - T_{su,min} - T_{flt_dq,max}]$$

EQUATION 2

$$Thld_mrg = [T_{co_dq,min} + (T_{clk_skw,max} + T_{pcb_skw,max}) - Thld,min + T_{flt_dq,min}]$$

With timing parameters as defined below:

T_{su_mrg} = Setup timing margin.

$Thld_mrg$ = Hold timing margin.

T_{cyc} = Clock cycle time (period).

T_{jtr} = Time variation in adjacent clock periods (jitter).

$T_{clk_skw,max}$ = Output clock buffer skew (maximum).

$T_{pcb_skw,max}$ = PCB flight time skew for clock traces (maximum).

$T_{co_dq,max}$ = Driver's data output valid delay (maximum).

$T_{co_dq,min}$ = Driver's data output valid delay (minimum).

$T_{su,min}$ = Receiver's input setup requirement (minimum).

$Thld,min$ = Receiver's input hold requirement (minimum).

$T_{flt_dq,max}$ = Signal flight time (maximum).

$T_{flt_dq,min}$ = Signal flight time (minimum).