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本文重点说明常用印刷电路板表面涂层的缺点。一些初始设备制造商使用表2和表3，根据印刷电路板技术识别适当的涂层。没有一种涂层能够满足所有应用的组装要求。本来银涂层最接近于扮演通用表面涂层的角色，但由于锈蚀产生的缺陷排除了这种可能性。其它表面涂层能够符合大部分制造和产品性能的标准，但很贵。这个讨论是从初始设备制造商的观点出发的，包括制造商所关心的问题。

# The Search for the Universal SURFACE FINISH

An evaluation of the advantages – and limitations – of common surface finishes. by MIKE BARBETTA

There are over a dozen surface finishes on the market. All are useful for some applications, but none really fit the category of “universal surface finish.”

This article will highlight each of the common surface finishes with regard to advantages and shortcomings, and itemize what is paramount to the PCB design community when choosing the correct finish for bare boards. My goal is to spark industry interest in resolving the technical issues surrounding existing processes and to develop new products.

My point of view is that of an OEM, though I also share concerns of fabrication and assembly. Finally, the paper will also discuss the industry needs going forward; especially regarding the tight pitch tendencies and higher speed requirements of future systems.

The surface finishes profiled are:

- HASL.
- OSP.
- ENIG.
- Immersion silver.
- Immersion tin.
- Electrolytic nickel-gold.
- Electroless nickel/palladium/immersion gold.
- Selective finishes.
- Reflowed tin-lead.

Certainly there are more products on the market than those listed above. However, they hold a relatively smaller market share and are not part of this article.

Each finish has distinct limitations restrict its use in other, expanded applications. The electronics design and manufacturing industry really needs two things from material vendors:

- A universal surface finish that satisfies all the requirements of the OEM.
- A surface finish that can be used in applications that reach

signal speeds in excess of 7 Gb/s.

OEM requirements for a surface finish can be divided into two groups:

#### Internal:

- Signal integrity.
- High-speed signal capacity.
- EMI shielding.
- RF capable.
- High joint strength.
- Contact resistance.

#### External:

- Cost, cost, cost.
- Shelf life.
- Whether it can be reapplied.
- Wetting/solderability.
- Good for 5-plus year end-of-life.

Also, the surface coating must not slow the signal speed of boards that run in excess of 7 Gb/s. Immersion silver is the only surface finish that satisfies this requirement without compromising any of the other necessary characteristics for a final finish (TABLE 1). However, tarnish after assembly is still a primary issue and it prevents silver from being used as universally as once hoped. Extensive testing of tarnished silver PCBs for loss of functionality has shown the deposit remains usable. EMI shielding, EMI leakage, contact resistance, signal integrity, solderability and joint strength have all been profiled in these studies. Despite the data for silver deposits, cosmetic issues remain the major cause for rejects. It is hoped that the new generation of tarnish-resistant silvers being tested will eliminate cosmetic tarnish on immersion silver plated PCBs.

TABLE 1. Advantages and Disadvantages of Common Surface Finishes

SURFACE FINISH	THICKNESS	ADVANTAGES	DISADVANTAGES
HASL	50-1500 µin	<p>“Nothing solders like solder.”</p> <p>Easily applied.</p> <p>Lots of industry experience.</p> <p>Easily reworked.</p> <p>Good bond strength.</p> <p>Withstands multiple thermal cycles.</p>	<p>Huge coplanarity differences resulting in off-contact printing and assembly defects.</p> <p>Contains lead.</p> <p>Not suited for high aspect ratios.</p> <p>Not suited for &lt; 0.020” pitch.</p> <p>PCB dimensional stability issues.</p> <p>Bridging problems on fine pitch assemblies.</p> <p>Inconsistent coating thicknesses (on varying pad sizes).</p>
OSP (Benzimidazoles)	0.2-0.6 µm	<p>Flat, coplanar pads.</p> <p>Reworkable (by fabricator).</p> <p>Doesn’t affect final hole size.</p> <p>Short, easy process.</p> <p>Cu-Sn IMC formed has been reported to be stronger and more robust than Cu-Sn from HASL and Ni-Sn from Ni-Au.</p>	<p>Assembly line changes may be required; not a drop-in.</p> <p>Question remains over reliability of exposed Cu after assembly.</p> <p>Limited thermal cycles.</p> <p>Cannot be reworked by assembler.</p> <p>Sensitive to some solvents used for misprint cleaning.</p> <p>Limited shelf life.</p> <p>Test pins cut coating, leaving exposed copper.</p>
ENIG	125-250 µin Ni 2-8 µin Au	<p>Planar surface.</p> <p>Consistent thicknesses.</p> <p>Withstands multiple thermal cycles.</p> <p>Long shelf life.</p> <p>Solders easily.</p> <p>Good for fine-pitch product.</p>	<p>Not wire bondable.</p> <p>Expensive.</p> <p>Should not be used on ≤ 1.0 mm pitch; black pad issues.</p> <p>Waste treatment of Ni.</p> <p>Cannot be reworked by fabricator.</p> <p>Ni is suspected carcinogen.</p> <p>Not optimal for higher speed signals.</p>
Immersion Ag	≥ 5 µin	<p>Good for fine-pitch product.</p> <p>Planar surface.</p> <p>No black pad concerns.</p> <p>Short, easy process cycle.</p> <p>Eliminates nickel.</p> <p>Doesn’t affect final hole size.</p> <p>Long shelf life.</p> <p>Can be reworked/reapplied by the fabricator.</p> <p>OK for multiple Insertions.</p> <p>Inexpensive.</p> <p>Drop-in process for the assembler.</p> <p>Good for ultra-high speed signals.</p>	<p>High friction coefficient; not be suited for compliant pin insertion (Ni-Au pins).</p> <p>Some systems cannot throw into blind vias with aspect ratios &gt; 1:1.</p> <p>Tarnishing must be controlled.</p>
Immersion Sn	25-60 µin	<p>Good for fine-pitch product.</p> <p>Planar surface.</p> <p>Eliminates nickel.</p> <p>Can substitute for reflowed solder in selective strip.</p> <p>Inexpensive.</p>	<p>Handling concerns.</p> <p>Panels need to be routed and electrically tested before coating.</p> <p>Contains thiourea.</p> <p>Limited rework cycles at assembler.</p> <p>Horizontal process needs nitrogen blanket.</p>
Electrolytic (hard) Ni-Au	50-200 µin Ni 5-50 µin Au	<p>Plated Ni-Au can be used as etch resist.</p> <p>Available for “mixed technology” products.</p> <p>Au wire bondable.</p>	<p>Exposed Cu sidewalls.</p> <p>Ni slivers after SES.</p> <p>Ni throwing power issues in small vias.</p> <p>Costly process.</p> <p>Excess Au easily plated on board edges causing poisoning of solder joints.</p>
Electroless Ni/Pd/Immersion Ag	120-240 µin Ni 10-30 µin Pd 3-8 µin Au	<p>Pd keeps Ni from passivating in presence of “porous” gold coating.</p> <p>Al wire bondable.</p> <p>Planar surface.</p> <p>Good for fine pitch product.</p>	<p>Additional processing step for fabricator (adds cost).</p> <p>Dip tank process.</p> <p>Evidence that Pd poisons solder paste after reflow.</p> <p>Waste treatment.</p>
SSS (Selective Solder Strip)	See applicable surface finishes	<p>Hot bar reflow for TAB devices.</p> <p>Viable alternative to HASL on thick product.</p>	<p>Multiple resist and photo cycles.</p> <p>Difficulty in controlling plated Sn-Pb thickness.</p> <p>Overlap (butt) line difficult to control.</p> <p>Expensive.</p>
Reflowed Sn-Pb	50-1500 µin	<p>Fast process.</p> <p>Inexpensive.</p> <p>Time tested.</p> <p>Good for solderability.</p>	<p>Solder slumping may cause hole size reduction-violation.</p> <p>Reflowing causes uneven deposit thicknesses in the hole.</p> <p>Heavy panels may require automated handling.</p> <p>Not a planar deposit.</p>

In our discussions on benefits and limitations of common surface finishes, it is important to note that the benefits and drawbacks of these deposits may vary according to fabrication and assembly processing and OEM applications. Immersion silver is a good example. For most OEMs, tarnish is not an issue because there is no exposed silver on the PCB after assembly. However, some OEMs use exposed edge rails and/or uncoated internal pads for NPTHs (non plated through-holes), and these can exhibit tarnish after assembly or burn-in.

Despite the many advantages and drawbacks of each surface finish, there are one or two major aspects that preclude its universal or widespread use:

#### HASL:

- Bridging of tight pitch outerlayer traces, and hole plugging on small through-vias.
- The lack of coplanarity is not the issue it was once thought. Reason: Newer, horizontal processors have minimized this effect, and assemblers' specifications usually permit a 0.003" standoff, making lack of coplanarity less likely to be a problem.

#### OSP:

- Lack of robustness of the deposit makes it difficult to rework or clean.
- Electrical test pins cut through the coating and expose potential corrosion sites.
- To eliminate the latter issue, many fabricators apply OSP after electrical test. This exposes the test bed to defects – such as copper voids in the hole due to overly aggressive OSP preclean microetch – that will not be identified until after assembly. By this point the value of the scrap rises exponentially.

#### ENIG:

- The rise of “black pad” defects, which cause massive solderability failures.
- Not suited for high-speed (>7 Gb/sec) applications; there is evidence that the nickel in the deposit slows down the signal speed.

#### Immersion silver:

- Tarnish causes many cosmetic failures for boards with exposed silver after assembly.
- Remaining UL limitations on its use.

#### Immersion tin:

- Lingering questions surrounding the growth of whiskers and dendrites over time, especially at room temperature.
- Some vendors' processes need a more vigorous deposit; some do not withstand multiple thermal cycles.

#### Electrolytic nickel-gold:

- Difficult to get the minimum 70 µin of nickel plated in the small thru-vias.
- Nickel slivers cause shorts across traces.
- Excess gold in high current density areas (HCDAs) causes gold embrittlement of the solder fillets.

#### Electroless nickel-palladium-immersion gold:

- For most OEMs the cost is excessive.

#### Selective solder strip:

- Expense for process too great. Most often used because there is no single surface finish that can satisfy all the requirements on the PCB. At best, an expensive compromise.

#### Reflowed tin-lead:

- Solder slumping causes hole size violations on thick backpanels.

### Surface Finish Selection

**TABLES 2** and **3** are used by some OEMs to identify the proper surface finish according to the technology of the boards. As can be seen, no single finish satisfies all the applications for assembly, even if we disregard the (odd) need for wire bonding. Again, silver comes closest to filling the role of universal surface finish, but defects caused by tarnish preclude that from being the case. Keep in mind that the few items that seem to pass the “universal surface finish” criteria have major cost concerns compared to the majority of the coatings listed.

Although the information contained herein breaks no new ground,

**TABLE 2.** Surface Finish Usability Based on Technology

SURFACE FINISH	THROUGH-HOLES	PRESS-FIT	SMT	FINE-PITCH BGA	EMI SHIELDS	CARD GUIDES	EDGE CONNECTORS	FLIP CHIPS	GOLD WIRE BOND	ALUMINUM WIRE BOND
Selective Solder	OK	OK	OK	OK	OK	OK	OK	OK	No	No
ENIG	OK	OK	OK	No <sup>1</sup>	OK	OK	OK	OK	No	No
HASL	OK	OK	OK	No	OK	OK	OK	No	No	No
Immersion Sn	OK	OK	OK	OK	OK	OK	OK	OK	No	No
Immersion Ag	OK	OK	OK	OK	No <sup>3</sup>	OK	OK	OK	No	No
OSP	OK	OK <sup>2</sup>	OK	OK	No	No	OK	OK	No	OK
Electrolytic Ni-Au <sup>4</sup>	No <sup>5</sup>	OK	OK	OK	OK	OK	OK	OK	OK	OK
Reflow Sn-Pb	OK	OK	No	No	OK	No	OK	No	No	No

<sup>1</sup>Not recommended for 1.0 mm pitch or less. <sup>2</sup>Not the best or more robust choice. <sup>3</sup>EMI shielding OK, but tarnish forms when left unsoldered/exposed. <sup>4</sup>Electrolytic Ni-Au will embrittle solder paste due to excess gold plated in PCB high current density areas. <sup>5</sup>Not for aspect ratios > 8:1 due to poor throwing power

**TABLE 3.** Attributes of Select Surface Finishes

	AG	ENIG	HASL	OSP
Coplanar deposit	Yes	Yes	No	Yes
Non-galvanic	Yes	No	Yes	Yes
Shelf life	12 months	12 months	9 months	6-9 months
Multiple rework cycles	Yes	Limited	Limited	no
Higher cost savings	Yes	No	No	Yes
CEM line changes needed	No	Yes	Yes	Yes
Doesn't reduce hole sizes	Yes	Yes	No	Yes
OK for ≤ 1.0 mm BGA pitch	Yes	No	No	Yes

we strongly believe that it needs periodic review to focus the need for a universal surface finish and improve existing processes, which in turn should ultimately lead to a paring of the number of surface finishes used.

This would be welcomed by fabricators, which could achieve significant cost savings by reducing the amount of employees needed for final finishing, and reducing chemistry and materials acquisition, floor space and utilities consumption.

Assemblers would also see substantial benefits. By reducing the number of different fluxes needed for all the surface finishes processed, there would also be set-up savings, and in some cases fewer process lines would be needed.

OEMs would benefit from the reduced number of surface finishes by not having to track which finish is applied to which part number (the same part number can have different finishes on multiple lots or date codes, in some cases). Logistically, much time and money is spent to organize, disposition and classify when each finish should be used. Funds can also be preserved by eliminating the expense of testing, studying and qualifying each surface finish on the market.

Finally, customers would benefit from having uniformity in the PCB coatings which make swaps, replacements and even reliability matches for the boards in their systems easier to track and predict. [PCD&M](#)

**MIKE BARBETTA** is a consultant with 25 years experience in PCBs. He has worked for Cisco Systems, Sanmina/Hadco, Shipley and MacDermid, among others. He can be reached at [mbarbetta@sbcglobal.net](mailto:mbarbetta@sbcglobal.net).