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若以每秒1吉字节或以上的速度在超过20英尺的距离上传输数据，可能会遇到问题。尽管10年前一般认为铜线的传输速率不能达到每秒2.5吉字节或以上，但现在很多公司都在使用同轴铜线印刷电路板（见图9），以每秒40吉字节的速率传输数据。实际上，铜线对于印刷电路板的数据传输率不构成基本的短期限制。相反，需要权衡的是成本和效率。对于较高的数据传输率，铜线互连能否提供上述传输率不成问题，关键是需要多少成本以及是否存在成本效率更高的系统方法。

## Has the Copper Interconnect Hit Its SPEED LIMIT?

Data rates are reaching the unlikely speed of 40 Gbps, yet copper runs on. by DR. ERIC BOGATIN

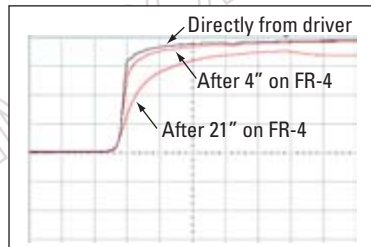
Let's get something straight. It's the silicon that does all the work. It's the silicon where the information is processed and stored, and the signals generated. Packaging and interconnects increase the product's size, weight, cost and time-to-market, while decreasing the signal quality. That's it. What a happy thought! Interconnect engineers can't increase system performance; at most, we try to minimize the hit.

This fact is never more apparent than in high-speed serial links, where the bandwidth of signals is ever increasing and the interconnect lengths extend across the entire board, even into large backplanes. We are pushing up against practical limits of data rates that can be transmitted over conventional copper interconnects.

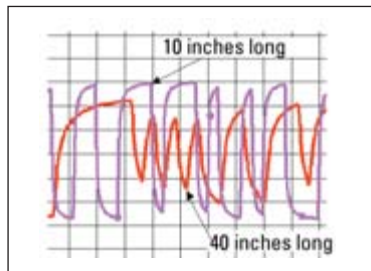
If special attention is not paid, problems may be encountered when transmitting high-speed serial links at data rates of 1 Gbps or more over lengths longer than 20". The biggest speed bump limiting the data rate of transmission is the increased rise time of the transmitted signal, an increase caused by the interconnect. **FIGURE 1** shows an example of the measured rise times of what originally is a 50 ps signal, propagating through FR-4 interconnects of 4" and 21".

If the slower rise time is as long as

the bit period, the received data pattern will be distorted. If the rise time increase is too high, the data pattern will be distorted beyond recovery. **FIGURE 2** is an example of a received 2.5 Gbps data pattern for two different lengths of interconnect. At 10", the data pattern is



**FIGURE 1.** Received signal directly from the driver, after 4" and 21" on FR-4. Initial rise time is 50 ps and time base is 200 ps/div. Measured with a GigaTest Probe Station and an Agilent 86100 DCA TDR.



**FIGURE 2.** A 2.5 Gbps bit stream through a 10" and 40" transmission line in FR-4, simulated with Mentor Graphics' Hyperlynx, 1 ns/div.

useful. At 40", it will probably result in errors. This rise time degradation is fundamentally due to two causes: losses in the interconnect from the conductor and the dielectric, and reflections from impedance discontinuities. Both factors cause less-high-frequency components of the signal to be transmitted. The losses absorb the high-frequency components, while the impedance discontinuities reflect the higher frequency components back to the source.

If each frequency component were affected in the same manner, the received signal would look the same as the original signal, just lower in amplitude. But if the higher-frequency components are preferentially blocked compared to the lower frequency components, the bandwidth of the transmitted signal will decrease and the rise time will increase.

As a rough order of magnitude estimate, the rise time degradation in a typical FR-4 interconnect is about 10 ps per inch of interconnect. For a 20"-long trace, the rise-time degradation from the interconnect alone can be about 0.2 ns. We usually call an interconnect with a rise-time degradation problem a "lossy" interconnect, or a lossy line.

Signals with a bit rate over 1 Gbps, or bit period shorter than 1 ns, and transported over lengths longer than

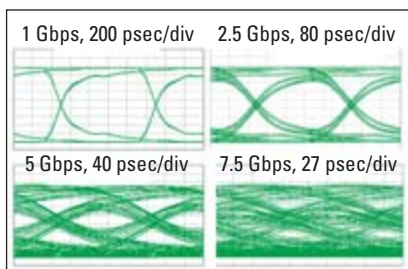
Serial ATA	1.25 Gbps
Hypertransport	1.6 Gbps
AGP8x	2.1 Gbps
Infiniband	2.5 Gbps
PCI Express	2.5 Gbps
Serial ATA II	2.5 Gbps
XAUI	3.125 Gbps
PCI Express II	5.0 Gbps
OC-192	9.953 Gbps
10 GbE	10 Gbps
OC-768	39.81 Gbps

**FIGURE 3.** Some of the current and next-generation high-speed serial link interfaces.

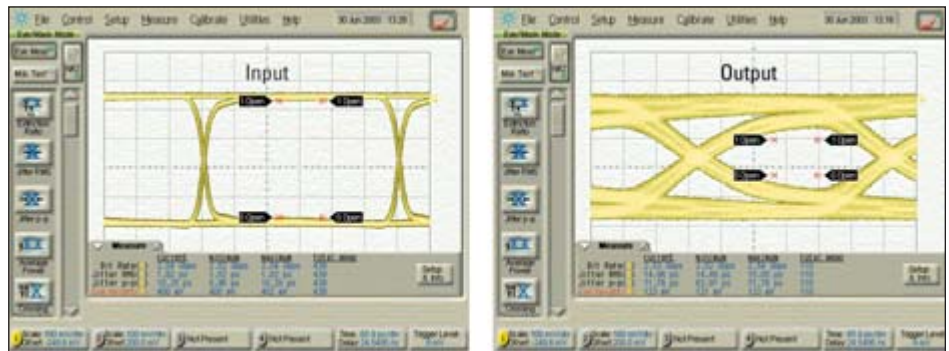
20", are sensitive to lossy line effects. All next-generation high-speed interface specs fall in this regime. **FIGURE 3** lists a number of these current or proposed specs. These high-speed serial links will challenge the materials and design choices for motherboards and backplanes.

When the rise time supported by the interconnect is comparable to or longer than the bit period, the received bit stream is distorted. The amount of distortion of one bit depends on the previous pattern. If there were a lot of 000's prior, the next 1 bit will not rise very high before it is pulled down. This effect of the current bit voltage level being dependent on the previous bit pattern is called intersymbol interference or ISI.

When ISI is strong, the voltage levels of one bit depend on the previous bits. We can display, at a glance, the impact on a single bit from all possible previous bit patterns. We take a long, received bit pattern and cut out each bit, synchronized with the clock. We superimpose each of these bits on top of each other. The resulting pattern looks like a human eye and we call this an eye diagram.



**FIGURE 5.** Eye diagrams for 26" long backplane differential channel measured with Agilent 4 port VNA and PLTS software with a GigaTest Probe Station.

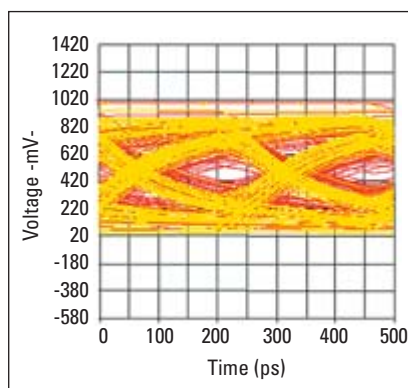


**FIGURE 4.** Eye diagram of 2.5 Gbps PRBP input signal and received signal after 26" through a backplane, measured with Agilent 7162 Bit Error Rate Tester and GigaTest Probe Station.

The bit stream we use as the source should have all combinations of bit patterns. On a practical basis, we use a pseudo random bit pattern (PRBP) to save time so we don't have to literally look at all possible patterns.

**FIGURE 4** shows the measured eye diagram for a 2.5 Gbps data stream, as measured from the source and after traveling through 26" of a backplane, including two daughtercards. The more ISI, the more collapsed the eye. In order for a receiver to be able to distinguish between ones and zeros, the eye must be opened far enough. How much depends on the noise margin of the receiver.

In addition, the width of the crossover region is a direct measure of the jitter in the received signal. We call this the "deterministic jitter." It must be included in all timing budgets. In general, for the same interconnect, the higher the bit rate, the more collapsed the eye and the larger the relative deterministic jitter. There is always a highest bit rate that can be transmitted through an interconnect while still maintaining a



**FIGURE 6.** A 2.5 Gbps eye diagram with 0.004" wide (red) and 0.008" wide (yellow) transmission lines, simulated with Hyperlynx.

large enough eye opening. This sets the limit to the highest bit rate that can be supported by the interconnect.

**FIGURE 5** shows the eye diagram for the same 26" trace in a backplane at four different bit rates. This interconnect cannot support a bit rate much higher than about 5 Gbps.

### Rise-Time Degradation

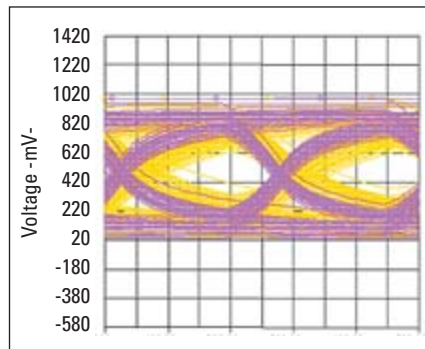
Two fundamental limits to the highest supported data rate are contributed by the interconnect – from the copper traces' resistance and the dielectric materials' dissipation factor.

The series resistance of the copper is frequency-dependent, due to skin depth effects. Increasing the thickness of the line has no impact on the series resistance. Only by making the line wider will the series resistance decrease. But to maintain an impedance of 50Ω, a wider line requires a thicker dielectric. There is a practical limit to how wide a copper trace can be used, of roughly 0.008".

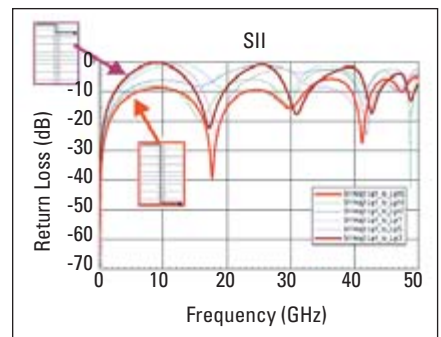
**FIGURE 6** shows the eye diagram of a 2.5 Gbps signal through a 40" long trace, with 0.004" wide and 0.008" wide traces. In general, to minimize the impact from conductor loss, use as wide a trace width as you can afford.

The property that affects dielectric loss is the dissipation factor of the material. In general, the dissipation factor is relatively constant over frequency. This term is a rough measure of the number of dipoles in the material and how easily they can move and absorb RF energy. A higher dissipation factor means more dipoles are available to suck up the electromagnetic fields and convert them into heat.

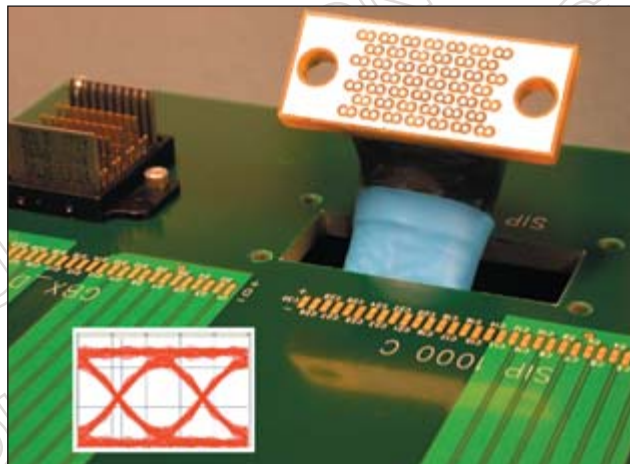
Even with a constant dissipation factor, the amount of attenuation will



**FIGURE 7.** A 2.5 Gbps eye diagram through a 40" transmission line with FR-4 (yellow) and low-loss laminate (purple), simulated with Hyperlynx.



**FIGURE 8.** Simulated return loss for different via designs, simulated with Ansoft's HFSS, (courtesy Ansoft Corp.).



**FIGURE 9.** Silicon Pipe coax backplane. Inset, a measured 40 Gbps eye diagram through one channel (courtesy Silicon Pipe, Agilent Technologies and TDA Systems).

increase with frequency. **FIGURE 7** shows the 2.5 Gbps eye for interconnects with a dissipation factor of 0.02, such as FR-4 and a low-loss laminate with a dissipation factor of 0.004. A lower dissipation factor laminate will mean less rise time degradation and less collapse of the eye diagram. Use as low a dissipation factor as you can afford.

Unfortunately, it is impossible to build a real motherboard or backplane without impedance discontinuities. In addition to the intrinsic losses in the uniform transmission line sections, there will also be impedance discontinuities whenever the geometry changes, such as at connectors, IC packages, termination resistors and vias.

Any impedance discontinuity will cause the higher-frequency components to be reflected back to the source, meaning they won't make it to the receiver. This will cause a rise-time degradation and collapse of the eye

diagram. In general, vias appear capacitive due to the capacitive coupling between the capture pads and long barrel and the interlayer ground planes.

Minimizing the impedance discontinuities is more often than not an issue of optimized design. A new generation of full-wave, 3D, electromagnetic field solver-based design and simulation tools predict impedance discontinuity before metal is cut and permit the design to be optimized for minimal discontinuity.

An example of simulating the return loss of a via, a measure of the impedance discontinuity, is shown in **FIGURE 8**. The goal is to make the return loss as large a negative dB as possible. This means a close match to 50Ω. The simulations illustrate how the specific layers the signal transitions between will strongly influence the size of the impedance discontinuity. Using such techniques, it is possible to optimize the via field design and minimize its impact on the eye diagram.

## 40 Gbps: The Limit?

Ten years ago, it was commonly believed that it might be possible to reach 1 Gbps across a backplane using copper traces, but 2.5 Gbps was just not going to happen. We would need optical interconnects beyond this data rate, according to conventional wisdom. But we pushed past the 2.5 Gbps data rate in copper. Then, the belief was that we might be able to get to 5 Gbps in copper, but couldn't possibly get to 10 Gbps. At this data rate and above, we would surely need optical interconnects.

Last year, Winchester Electronics announced routine transmission rates of 10 Gbps over copper. Analysts said, surely we will need optical interconnects to get to 40 Gbps. In 2003, Silicon Pipe announced a new type of backplane technology capable of 40 Gbps, based on a copper coax backplane (FIGURE 9). This data rate is at the limit of what can be measured using existing test equipment. Their technology uses wide conductors, but in a coax geometry, low-loss dielectric and well-matched connectors to daughtercards. This may represent the ultimate practical limit to the data rate in copper. Just judging from the 40 Gbps eye, it is clear we will have to wait for a new generation of measurement instruments to find how far above 40 Gbps this new technology can go.

The problem with copper interconnects is the frequency-dependent loss which degrades the rise time. If we know how the frequency components may be degraded, we can do some signal processing in the silicon to compensate. There are three commonly used techniques to improve the data transmission rates in the silicon. Each of these techniques is currently incorporated in specialized backplane driver chips called SERDES, or serializer-deserializer chips. As a general rule, implementing one or more of these features in silicon costs more money than not using them.

Pre-emphasis is a technique of adding extra high-frequency components so that by the time the signal is received, these added high-frequency components are the only things attenuated away, and the received spectrum matches the desired spectrum.

Equalization is a technique that attenuates the low-frequency components so

that the shape of the received spectrum is the same as the initial spectrum; it's just uniformly reduced across the entire bandwidth. The rise time is maintained.

Pulse amplitude modulation (PAM) is a technique of using multiple voltage levels to represent a bit. If 4 bits can be encoded using different voltage levels within one bit period, it's possible to use a lower clock frequency to transmit the same data rate. A lower clock frequency will be subject to less interconnect rise-time degradation.

Copper does not pose a fundamental, near-term limit to backplane data rates. Instead, there are cost/performance tradeoffs. Every feature that increases the data rate through copper interconnect adds to the cost of the backplane. Wider traces mean thicker boards. Lower dissipation factor laminates cost more. Higher bandwidth connectors, IC packages and termination components are more expensive. For higher data rates, it's not a question of whether a copper based interconnect can provide this but how much it will cost and whether more cost-effective system approaches exist. Every system will have a different set of tradeoffs between data rate, cost, risk and time-to-market. **PCD&M**

## REFERENCES

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